460 and signal 2 105 through sense signal 465. Sensing and delay circuit B 450 senses signal 2 105 through sense signal 470, signal 3 110 through sense signal 475, and signal 4 135 through sense signal 480. Sensing and delay circuit C 455 senses signal 4 135 through sense signal 485 and signal 5 140 through sense signal 490. The use of sensing and delay circuit 425, in particular sensing and delay circuit 450 and tri-state buffer 410 to delay signal 3, provides a uninterrupted continuous delay. Delay signal 435 is provided to tri-state buffer 410 whenever the delay actually is required to take place. This prevents separate delay glitches that can cause aberrations in signal transmission.

A4 CONT

In the Claims

The following is a clean version of the entire set of pending claims (unamended claims appear in smaller print). In accordance with 37 CFR § 1.121(c)(1)(ii), attached is a marked up version of claims containing the newly introduced changes. The attached page is captioned **VERSION WITH MARKINGS TO SHOW CHANGES MADE.**

Please add the following new claims:

A5

46. (New) An apparatus comprising:

a circuit configured to detect a transition of a first signal and a transition of a second signal and provide a delay signal when the transitions of the first and the second signals occur simultaneously; and

a first buffer coupled to the circuit, wherein the first buffer is configured to delay the transition of the first signal in response to the delay signal.

47. (New) The apparatus of claim 46, wherein the first buffer is configured to delay the transition of the first signal until the transition of the second signal has completed.

48. (New) The apparatus of claim 46, wherein

the circuit is further configured to detect a transition of a third signal and provide the delay signal when the transitions of the first and third signals occur simultaneously.

49. (New) The apparatus of claim 48, wherein the first buffer is further configured to delay the transition of the first signal until the transition of the third signal has completed.

A5

50. (New) The apparatus of claim 48 further comprising:

a second buffer configured to receive the second signal and provide a delayed second signal, wherein a delay of the second buffer is equal to an inherent delay of the first buffer; and

a third buffer configured to receive the third signal and provide a delayed third signal, wherein a delay of the third buffer is equal to the inherent delay of the first buffer.

51. (New) The apparatus of claim 50 wherein the first signal is adjacent to the second signal and the third signal.

52. (New) The apparatus of claim 50 further comprising:

CONT

a first sense signal, wherein the first signal is coupled to the circuit via the first sense signal;

a second sense signal, wherein the second signal is coupled to the circuit via the second sense signal; and

a third sense signal,wherein the third signal is coupled to the circuit via the third sense signal.

53. (New) The apparatus of claim 46 further comprising:

an integrated circuit coupled to the circuit.

54. (New) An apparatus comprising:

a circuit configured to detect a transition of each signal of a plurality of signals and provide a delay signal when any adjacent signals simultaneously transition; and

a plurality of buffers coupled to the circuit, wherein at least one buffer of the plurality is configured to delay at least one transition in response to the delay signal.

55. (New) The apparatus of claim 54, wherein the at least one buffer is configured to delay the at least one transition until all adjacent transitions to the at least one transition have completed.

AS

56. (New) The apparatus of claim 54, further comprising:

a first circuit configured to detect a transition of a first signal and a transition of a second signal and provide a first delay signal when the transitions of the first and second signals occur simultaneously; and

a first buffer coupled to the first circuit, wherein the first buffer is configured to delay the transition of the first signal in response to the first delay signal.

57. (New) The apparatus of claim 56, wherein the first signal is adjacent to the second signal.

58. (New) The apparatus of claim 57, wherein in response to the first delay signal the first buffer is further configured to delay the transition of the first signal until the transition of the second signal has completed.

CONT

59. (New) The apparatus of claim 56, further comprising:

a second circuit configured to detect a transition of the second signal, a transition of a third signal, and a transition of a fourth signal and provide a second delay signal when the transition of the third signal occurs simultaneously with at least one of the transition of the second signal and the transition of the fourth signal; and

a second buffer coupled to the second circuit, wherein the second buffer is configured to delay the transition of the third signal in response to the second delay signal.

60. (New) The apparatus of claim 59, wherein the third signal is adjacent to the second signal and the fourth signal.

61. (New) The apparatus of claim 59, wherein in response to the second delay signal the second buffer is further configured to delay the transition of the third signal until the transition of at least one of the third signal and the fourth signal has completed.

62. (New) The apparatus of claim 59, further comprising:

a third circuit configured to detect a transition of the fourth signal and a transition of a fifth signal and provide a third delay signal when the transitions of the fourth and fifth signals occur simultaneously; and

A5

a third buffer coupled to the third circuit, wherein the third buffer is configured to delay the transition of the fifth signal in response to the third delay signal.

63. (New) The apparatus of claim 62, wherein the fourth signal is adjacent to the fifth signal.

64. (New) The apparatus of claim 62, wherein in response to the third delay signal the third buffer is further configured to delay the transition of the fifth signal until the transition of the fourth signal has completed.

CONT

65. (New) The apparatus of claim 62 further comprising:

a fourth buffer configured to receive the second signal and provide a delayed second signal, wherein a delay of the second buffer is equal to an inherent delay of the first buffer; and

a fifth buffer configured to receive the fourth signal and provide a delayed fourth signal, wherein a delay of the fifth buffer is equal to the inherent delay of the third buffer.

66. (New) The apparatus of claim 54, further comprising:

a second circuit configured to detect a transition of each signal of a second plurality of signals and provide a second delay signal when any adjacent signals simultaneously transition;

A5

a second plurality of buffers coupled to the second circuit, wherein at least one buffer of the second plurality is configured to delay at least one transition in response to the second delay signal; and

CONT

a shield line between the plurality of signals and the second plurality of signals.